please insert the paragraph between the title and the first paragraph.

K.N.
11/19/04

DRY ETCHING WITH REDUCED DAMAGE TO MOS DEVICE

-- CROSS - REFERENCE TO RELATED APPLICATION

This application is a divisional application which claims the benefit of U.S. Patent Application Serial No. 08/787,451, filed on January 22, 1997, now U.S. Patent No. 6,376,388 B1, issued April 23, 2002, which is a continuation application of U.S. Patent Application Serial No. 08/275,426, filed on July 15, 1994, now abandoned. The disclosures of the prior applications are hereby incorporated herein in their entirety by reference. --

BACKGROUND OF THE INVENTION

a) Field of the Invention

The present invention relates to a semiconductor device and its manufacturing method, and more particularly to a semiconductor device having insulated gate type field effect transistors (IGFET) fabricated at a high integration.

b) Description of the Related Art

As patterns of large scale integration (LSI) circuits are becoming finer, it is desired to improve a pattern transfer precision. Anisotropic dry etching such as reactive ion etching (RIE) and electron cyclotron resonance (ECR) plasma etching is widely used so as to reliably transfer a mask pattern on a layer such as a wiring layer to be processed. Such anisotropic dry etching uses plasma or ions.

A plasma process is likely to produce an electrical stress such as a damage caused by non-uniformity of plasma (refer to J. Appl. Phys. 72 (1992) pp.4865 - 4872). As patterns are becoming finer, the gate insulating film of an insulated gate type field effect transistor (IGFET) is becoming thinner. There are many gate insulating films which have a thickness of 10 nm or less and are susceptible to influences and damages by an electrical stress. For example, if a Fowler-Nordheim (FN)